MOTOROLA

AN917
Application Note

READING AND WRITING IN FLOPPY DISK SYSTEMS USING MOTOROLA INTEGRATED CIRCUITS

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The floppy disk system has become a widely used means for storing and retrieving both programs and data. A floppy disk drive requires precision controls to position and load the head, and well defined read/write signals, in terms of amplitude and timing, in order that a viable system may result. This application note will deal with the read and write data paths, including head control and erase circuitry.

INTRODUCTION

This application note will initially discuss recording heads, formats, and disk capacities. Subsequently, the discussion will focus on the MC3469, MC3470, and MC3471 Integrated circuits, which have been developed to facilitate the design of a floppy disk system.

THE HEAD

The reading, writing, and erase functions are performed by a head consisting of a core, with a small air gap, and a set of windings. A typical head schematic is shown in Figure 1. This configuration (whereby one head performs the three functions) eliminates problems due to misalignment of individual heads, as well as saving space.

During recording, current in the R/W windings generates a magnetic field (flux) in the air gap, which in turn orients magnetic domains in the particles on the surface of the disk. The WRITE electronics directs current alternately to the two R/W coils, which are phased to produce opposite polarity magnetic fields at the air gap. The recorded data, which will be described in more detail later, is contained in the resulting pattern of flux **reversals**.

During reading, the changing pattern of the magnetic domains on the disk surface induces a voltage in the R/W windings, via the air gap/core combination. The voltage waveform from the head is then converted to pulses by the read chain electronics. The resulting pattern corresponds to the original written data.

The erase coil is activated, during writing, to trim the track to a desired width. The trim creates low noise guard bands between tracks by eliminating outward flux fringing, thus providing a cleanly written track, and reducing the effects of subsequent diskette and head position errors. The erase function is not meant to erase previously written data. That is accomplished by the R/W coils in that new data overwrites old data.

The dimensional stability of the core, air gap, disk diameter and flatness, head-to-disk height, head position, and head interface electronics are some of the critical factors which determine the performance and reliability of a floppy disk system.

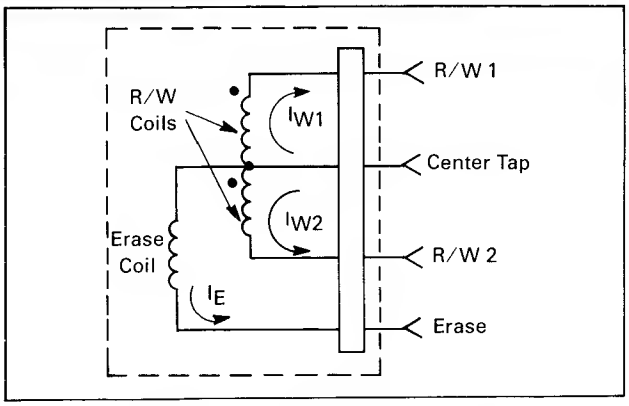


FIGURE 1 — Typical Head Configuration

There are two basic head types in common use. Figure 2 depicts the difference between the straddle erase head and the tunnel erase head. In the straddle erase head, each side of the read/write core incorporates an erase core whose gap (and flux) is perpendicular to the read/write gap. The tunnel erase head employs two erase cores mounted behind the read/write gap and core. The erase core flux is parallel to that of the read/write core.

Because of the physical positioning of the erase core, with respect to the R/W core, the erase enable timing differs for the two heads. For the straddle erase head, write and erase operations occur simultaneously. For the tunnel erase head, the erase function is activated a period of time after the writing begins, and is held active for a period of time after the writing is complete to compensate for physical displacement of the erase gap downstream from the R/W gap. The timing of the erase turn-on delay is based on this displacement, as well as the linear velocity of the outer most track (Track 00). The turn-off delay is generally slightly longer to account for the slower linear velocity of the inner most track.

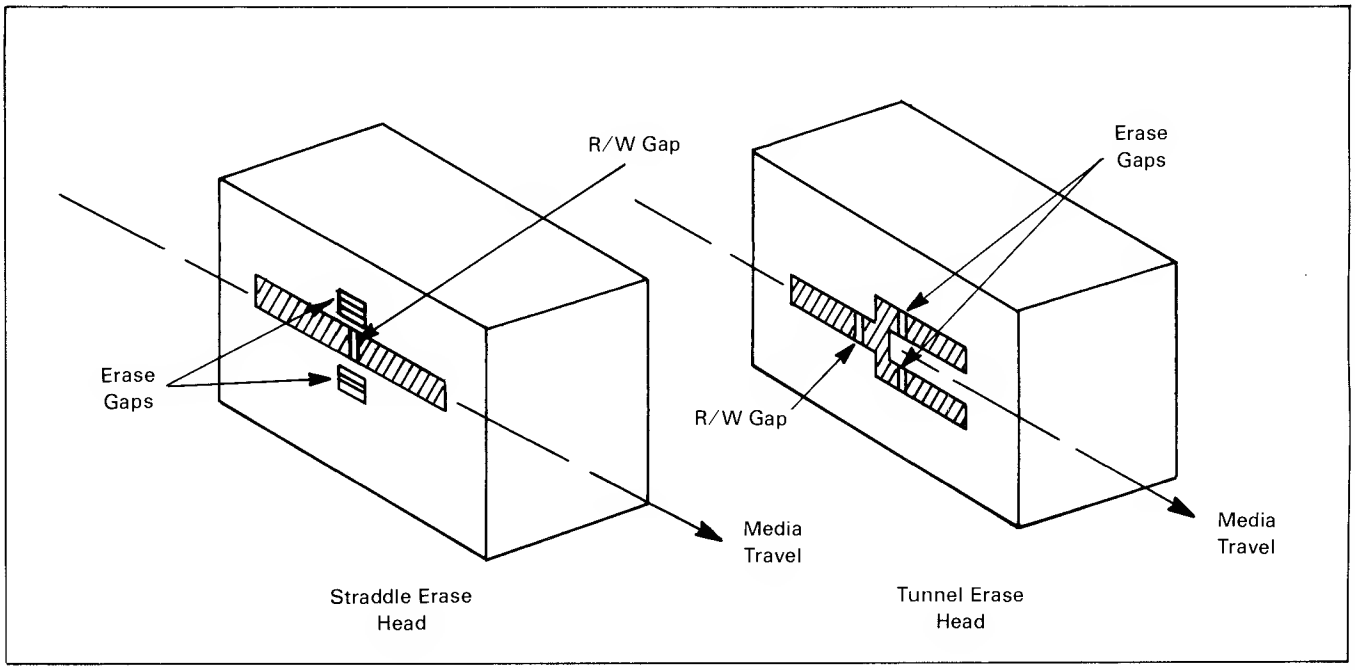


FIGURE 2 — Head Types

RECORDING INFORMATION

When magnetically recording digital information, the information is stored not in the amplitude or direction of magnetism on the media, but in flux reversals. Each bit of information in the original data is ultimately recorded in the form of a flux change, the direction of which is irrelevant.

To write digital data onto the magnetic medium, the data must be converted into head current and steered by circuitry that produces alternating direction saturated recording. The technique involves magnetically saturating the core with, ideally, 100% alignment of the magnetic domains on the disk by applying sufficient current to the R/W windings. This results in the maximum desirable flux amplitude applied to the disk surface, and additionally, prevents residual dc biasing of the core.

A typical waveform conversion, where the data pattern is first converted to FM pattern (to be described later), is shown in Figure 3. Each pulse in the FM pattern causes the head current to be switched from one R/W coil to the other, thus producing a pattern of flux transitions on the disk. Since only the flux transition is relevant, the initial direction of the head current is not important.

A simplified circuit for controlling the write current for a floppy disk head is shown in Figure 4. For the purpose of this discussion, the head center tap (CT) will be at a positive voltage (V_{BB}) for writing ("Write High"), and at ground for reading ("Read Low").

The opposite arrangement could be used just as well. The $\overline{\text{WRITE GATE}}$ input must be enabled (Logic "0") to permit writing on the disk. Each pulse of the FM data waveform (Figure 3) is applied to the $\overline{\text{WRITE DATA}}$ input, causing the flip-flop to toggle, thus switching the head current to the alternate R/W coil. The Erase Control block is enabled during this time, although the specific timing of this block depends on the type of head used, and will be discussed in more detail later.

When the writing is completed, or data is to be read, the $\overline{\text{WRITE GATE}}$ input is disabled (Logic "1"), which stops current flow in the three head coils. (The Motorola Read and Write ICs to be discussed later, use the Write High, Read Low method.)

RECOVERING INFORMATION

The data recovery technique, and circuitry, is somewhat more involved than that used for recording the information, due to the low (millivolt level) signal produced by the read head. The signal must be converted to digital pulses, while ignoring the effects of noise and positional errors present in any system. The read operation is performed with the same windings used for writing. The center tap, however, is pulled to the level opposite that used for writing (to Gnd in Figure 4).

As the flux transitions pass under the head gap, a voltage is induced in the R/W windings. The voltage is the derivative of the magnetic flux pattern, as given by:

$$E = N \frac{d\phi}{dt}$$

Thus, flux transitions, which were produced by the data pulses (during writing), will generate the peaks of the head output voltage. The read circuitry must convert the voltage peaks into data pulses. A simplified block diagram, as shown in Figure 5, is composed of a preamplifier, filter, differentiator, zero-crossing detector, time domain filter, and pulse generator.

The preamplifier is required since the signal from the head is usually 2-20 mV. A typical gain of 100 brings the signal up to a usable level. The balanced low-pass filter attenuates noise and unwanted harmonics. The balanced differentiator converts the peaks into zero crossings. The zero crossing detector triggers the time domain filter and pulse generator to produce the output pulses. Figure 6 shows a typical read signal, the differentiated signal, and the resulting data.

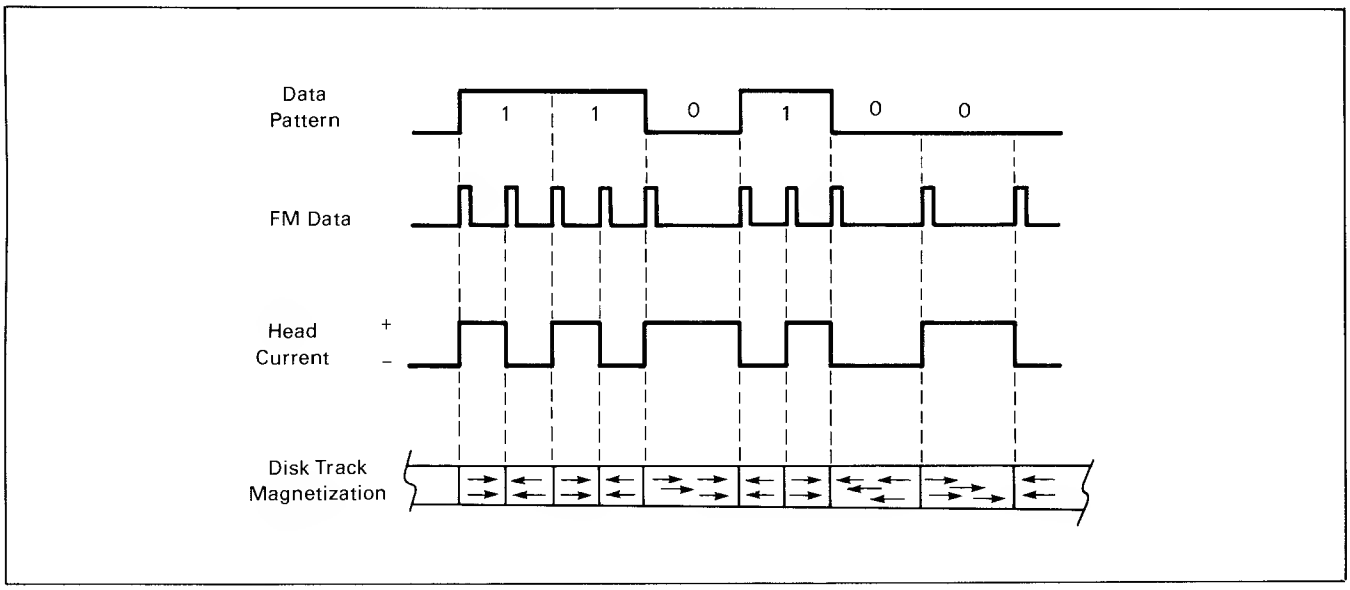


FIGURE 3 — Saturation Recording

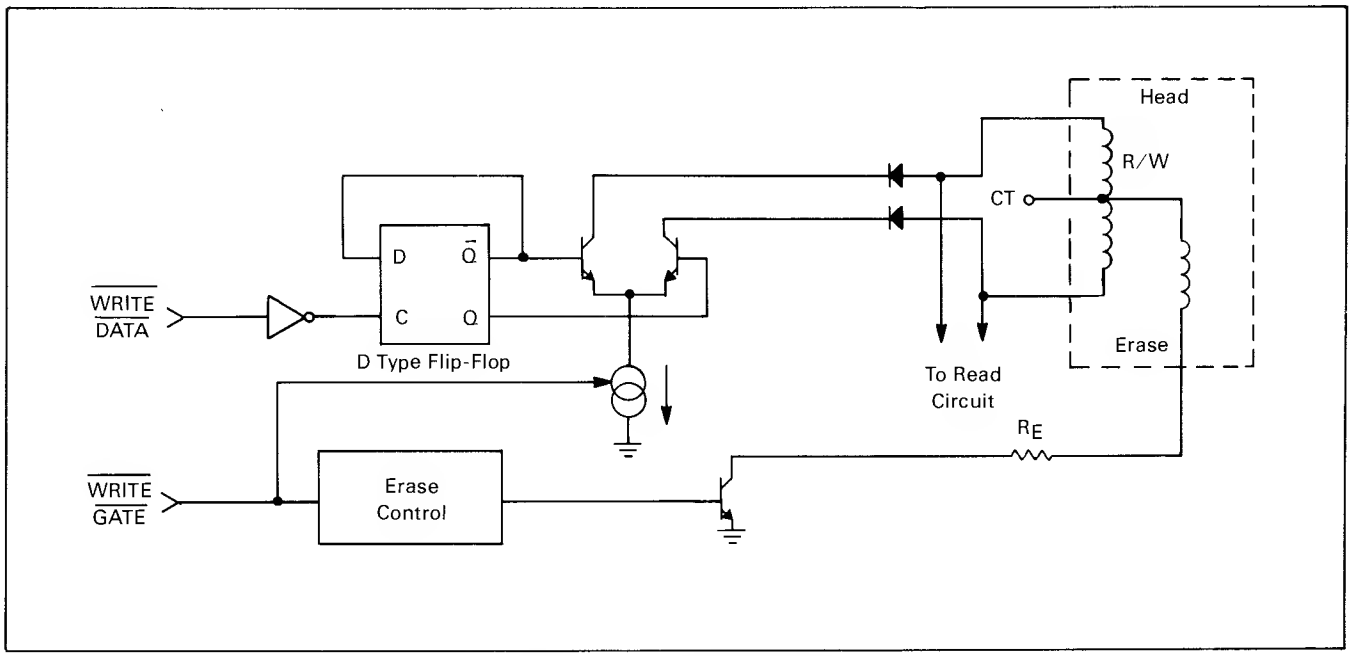


FIGURE 4 — Simplified Write Circuit

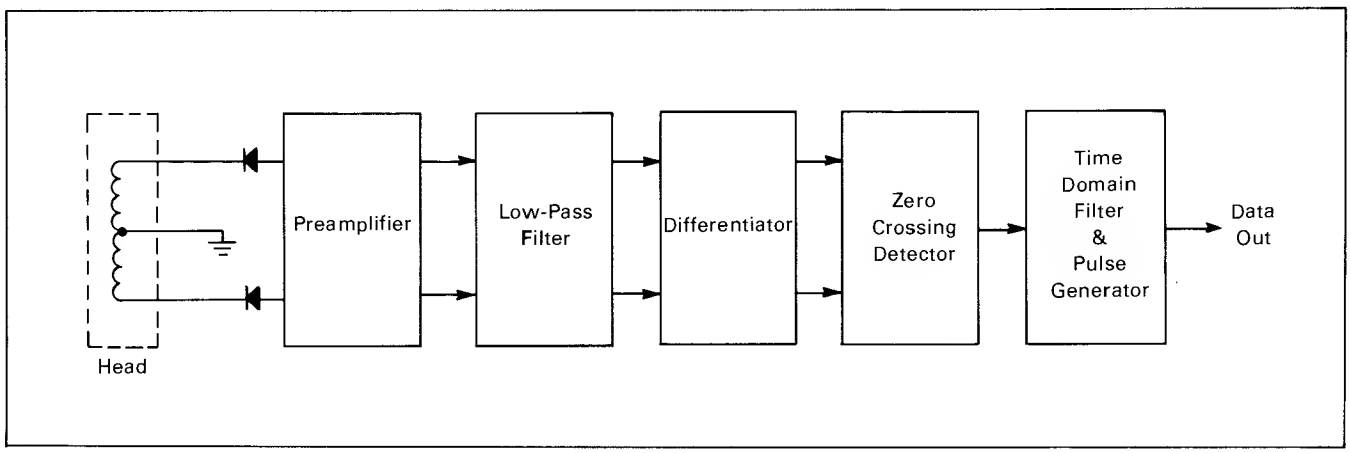


FIGURE 5 — Data Recovery Block Diagram

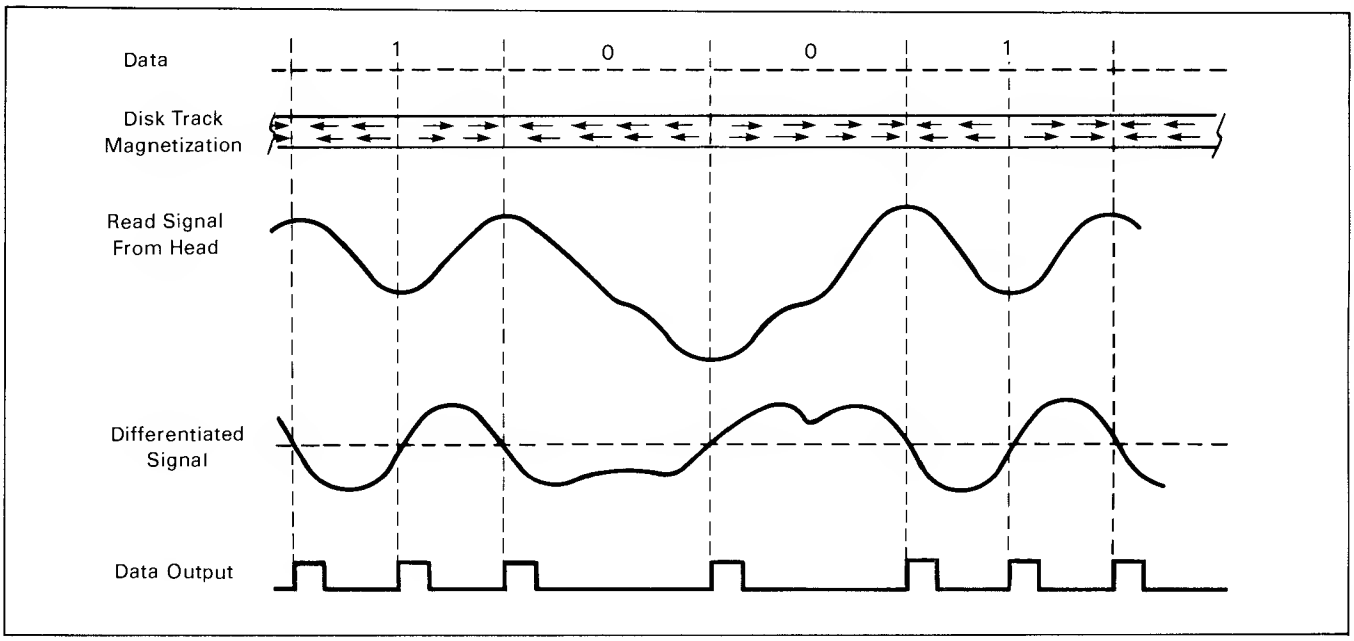


FIGURE 6 — Read Signal Characteristics

RECORDING FORMATS

There are, at present, two industry standard formats for recording a serial bit-stream onto a floppy disk. The first to be used, frequency modulation (FM), is based on the IBM 3740 method of encoding. This format produces a so-called "single density" capacity. The double density capacity is realized by using one of several more complex encoding schemes, the most popular scheme being Modified Frequency Modulation (MFM). A comparison of the two schemes will show how the greater capacity is realized.

FM recording (see Figure 7) involves writing a clock pulse at the beginning of each bit-cell (4.0 μs wide),

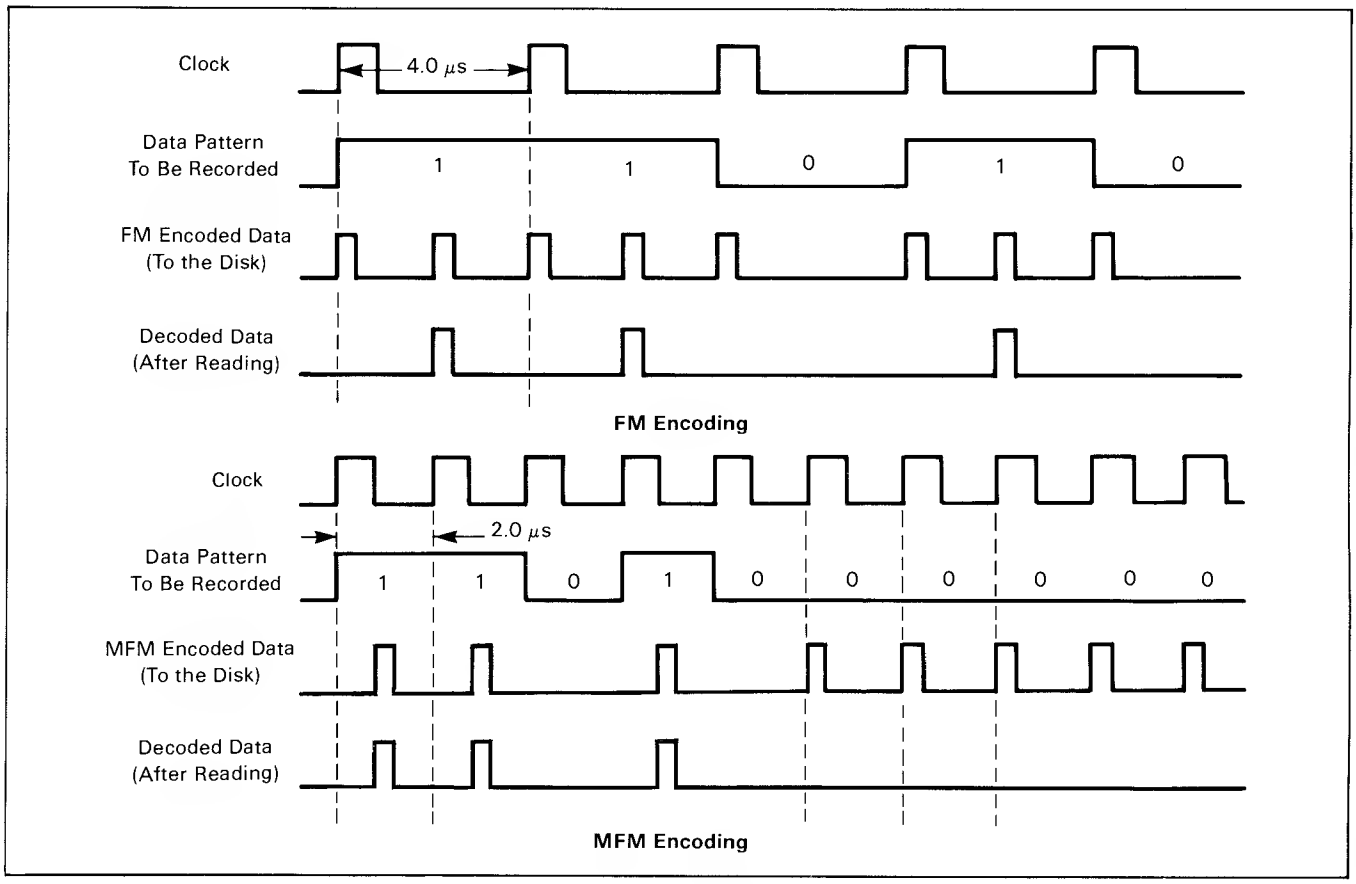


FIGURE 7 — Recording Formats

and then writing a pulse at the center of the bit-cell if the data is a Logic "1". A Logic "0" results in the absence of a pulse at the center. This technique therefore requires the allowance for two flux changes on the disk per bit-cell. In this scheme, the clock pulses provide the timing reference for both writing and reading.

MFM encoding doubles the data capacity by eliminating the need for clock pulses at the beginning of **every** bit cell. Clock pulses are needed only when data pulses (representing a Logic "1" bit) are not present in both the preceding and the current bit-cell. The size of the bit-cell is reduced to 2.0 μs, thereby doubling the transfer rate, and the disk capacity. Clock pulses are written at the **beginning** of the bit-cell, while data pulses are written at the **center** (see Figure 7). This scheme results in one flux change per bit-cell.

Separation of clock and data pulses (during reading of either above format) is handled by the host controller, and commonly employs the use of a phase-locked loop circuit.

DISK CAPACITIES

The currently available standard floppy disk sizes are 8 inch diameter, and 5¼ inch diameter (mini-floppy). [Other disk sizes (2", 3", 3¼", 3½", etc.) are available, and standards for these are currently being developed.] The size difference, as well as different recording patterns, between the 5¼" and 8" diskette, provide for a recording capacity difference of three to one. The 8" floppy has a data transfer rate of 250 kHz for FM recording and 500 kHz for MFM recording. The mini-floppy (5¼") has transfer rates of 125 kHz and 250 kHz, respectively.

Originally, the standard for track densities was 48 tracks per inch (TPI) with a track width of 0.012 or 0.013 inch. This produced a guard band of approximately 0.008 inch (8.8 mils) between tracks. (See Figure 8.) While this standard is still used today, it is no longer dominant. 96 TPI is widely accepted, while densities of 100, 135, 150, and 170 TPI are used by several manufacturers.

The IBM 3740 format for soft-sectored*, single density 8 inch disks consists of 77 tracks of 26 sectors each, with 128 bytes (1024-bits) per sector for FM recording, providing a disk capacity of 256,256 bytes. The mini-floppy records FM data on 35 tracks, at 18 sectors per track, and 128 bytes per sector, providing a disk capacity of 80,640 bytes.

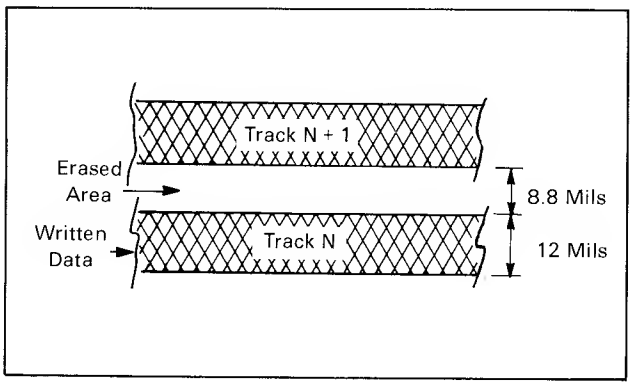


FIGURE 8 — Track Dimensions (48 TPI)

For double density (MFM) recording, the sector capacity is increased to 256 bytes, giving disk capacities of 512,512 bytes and 161,280 bytes, respectively.

Further capacity increases are constantly sought after by users (naturally), and consequently by manufacturers of disk systems, primarily to reduce the "cost-per-bit" factor. Other advantages include increased reliability (less disks to handle), and easier programming of the host system. Increasing bit densities involves increasing the bits per inch (BPI) written on the track (currently 2000–10,000 BPI), and increasing track density (TPI). As bits are packed closer and closer, however, the problems to be dealt with include decreasing signal-to-noise ratio, decreasing signal amplitude during reading, and increasing cross-talk from track-to-track, and bit-to-bit. While improvements in electronics can partly compensate, a great deal of emphasis is being put on improving the disk and the head assembly. Areas being investigated include:

- Thinner coating on the disk surface (allowing greater BPI);
- Greater uniformity of the coating;
- Tighter tolerances on the head assembly;
- Reduced R/W gap length (typically 80 micro-inches);
- Thin-film heads, using semiconductor manufacturing techniques;
- Use of lasers;
- Improving head positioning mechanisms (micro-inch tolerances are required).

*Soft-sectoring refers to the concept whereby the sector size, and consequently, the number of sectors per revolution are selectable by the system designer. Determination of sector size, and formatting of information, are typically done by the disk controller. Hard-sectoring, on the other hand, refers to an older and less popular system where the sector size is determined at the time the disk is manufactured by a set of unalterable index marks.

WRITE CONTROLLERS — MC3469,MC3471

To conserve PC board space, and increase reliability, Motorola has developed two integrated circuits (the MC3469 and MC3471), each of which replace, in expanded form, most of the circuitry of Figure 4. The two ICs differ only in the erase control circuit. The MC3469 and MC3471 perform the basic function of directing the write current alternately to the two R/W coils in response to the data pulses at the $\overline{\text{WRITE DATA}}$ ($\overline{\text{WD}}$) input. The write current is controlled (±3%) by an accurately trimmed current sink, referred to an external resistor (R_{ext}) according to the curve of Figure 10 which follows the relationship:

$$I_{write} = \frac{30}{R_{ext}}$$

(I in mA, R_{ext} in kΩ). Each IC is capable of controlling two heads. The MC3469 is optimized for use with straddle erase heads. The MC3471 can be used with either straddle erase or tunnel erase heads, since it provides both erase delay, and a read/step inhibit output while the head is active. See Figure 9.

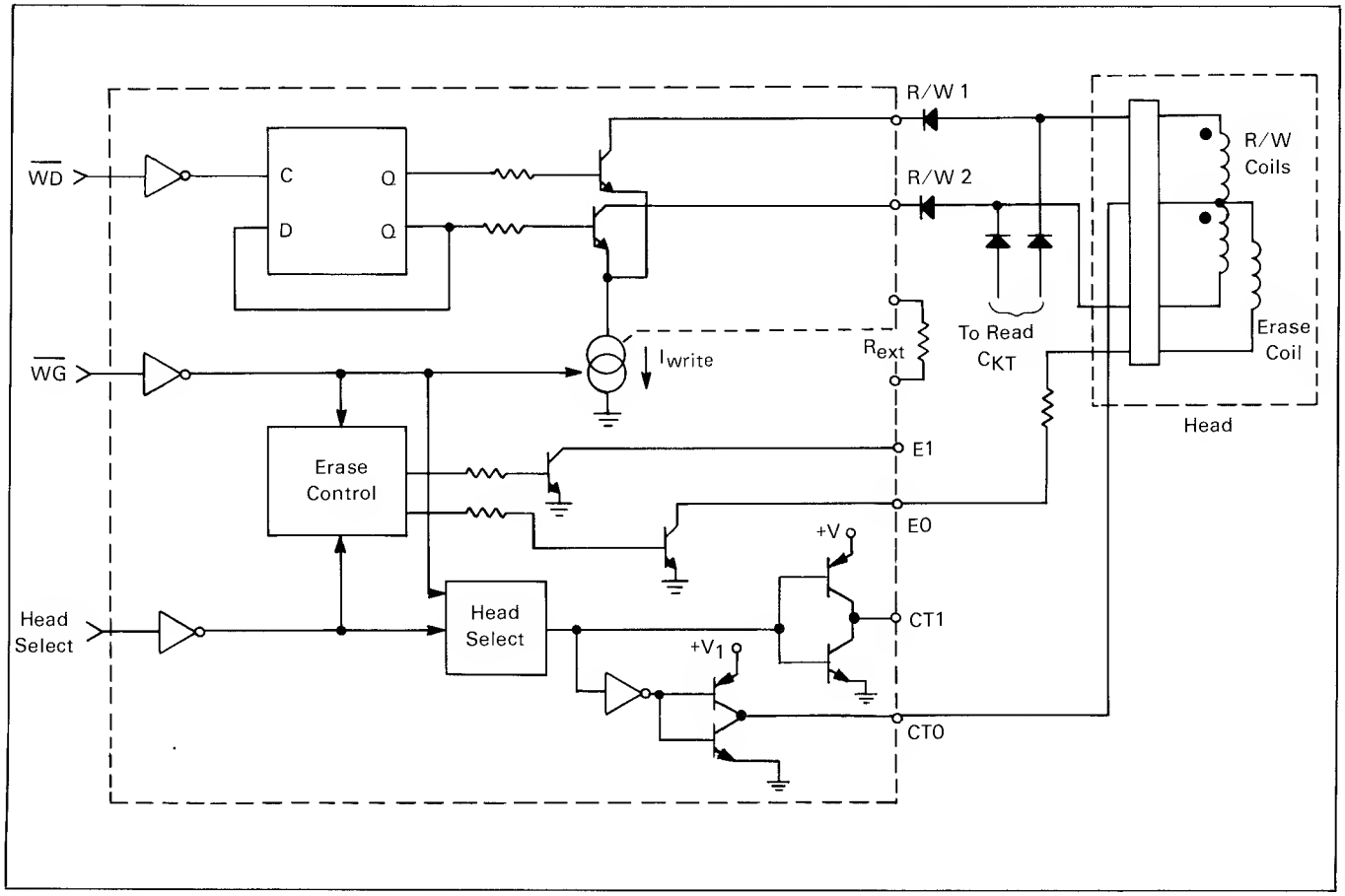


FIGURE 9 — MC3469/MC3471 Simplified Circuitry

NOTE: E1 and CT1 provide for operation of a Second Head.

Figures 11 and 12 show typical applications of the MC3469 and MC3471 in which two heads are controlled. A description of the various functions follows:

a) The IRWS input (when at a Logic "1") provides a head current increase, relative to Figure 10, of 33% for the outer tracks of the disk. This form of track compensation is not used by all disk drive manufacturers, since it is common mainly in 8" drives. This change is usually made between tracks 42 and 43.

b) It is in the erase feature that the MC3469 and MC3471 differ. The MC3469 enables and disables the selected center-tap output, and erase output, concurrent with the edges of $\overline{\text{WRITE GATE}}$ ($\overline{\text{WG}}$). The MC3471 has provisions for independently delaying the turn-on and turn-off of the erase coil current using either external RC networks, or logic gates. Typical applications require a turn-on delay of 500 μs, and a turn-off delay of 1.0 ms. R1 and C1 (Figure 12) establish the turn-on delay of the selected erase output E0 or E1 (selected by the Head Select input). R2 and C2 establish the turn-off delay of the selected erase and center-tap outputs. Both time delays are determined by $t = RC$. Figure 13 shows the two delays referenced to $\overline{\text{WG}}$. By using a ±5% capacitor, and a ±1% resistor, the delays are guaranteed to a ±15% accuracy. By tying the erase control pins (11 and/or 12) of the MC3471 to V_{CC} through pull-up resistors (no capacitors), the erase circuit functions identically to that of the MC3469.

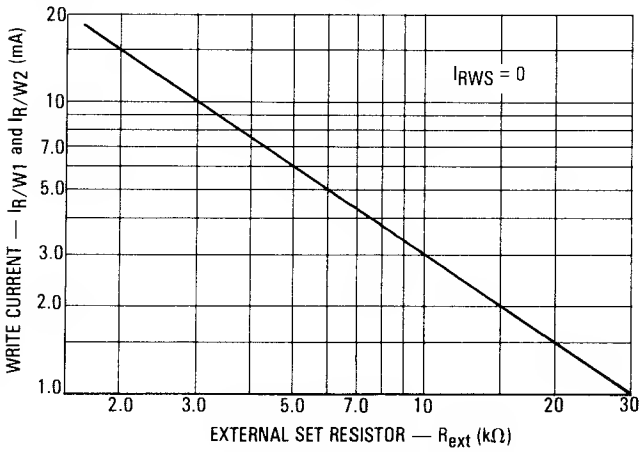


FIGURE 10 — Write Current versus R_{ext}

An alternative method of erase delay control is to connect a TTL or CMOS gate with an open-collector output, and a pull-up resistor, to the appropriate delay input. The delay input (D1 and/or D2) is held low until the respective desired time has lapsed. Releasing the input (low-to-high transition) allows the erase output to make its respective transition (following the appropriate $\overline{\text{WG}}$ transition). This method, shown in Figure 14, allows control from a microprocessor, or other logic control circuit. The rules to follow for signal lines G1 and G2 are as follows:

G1 — "Don't care" while $\overline{WG}$ is high;
Must be high when $\overline{WG}$ changes from high-to-low;
Must stay high for turn-on delay — then change to low;
Must stay low until after $\overline{WG}$ goes high.

G2 — Must be low while $\overline{WG}$ is high (prior to writing data);
"Don't care" while $\overline{WG}$ is low;
Must be high when $\overline{WG}$ changes from low-to-high;
Must stay high for turn-off delay — then change to and stay low.

c) As a result of providing erase turn-on/turn-off delays, an $\overline{INHIBIT}$ output was required for the MC3471. The output can be used (externally) as a synchronizing signal to inhibit reading, stepping, or other operations until writing, erasing, and degauss are completed. R3 (Figure 12) is the pull-up resistor for this open-collector, active low output which can be wire-OR'd with other signal outputs. See Figures 13 and 14 for timing.

d) The value of R_E (RE0 and RE1 in Figures 11 and 12) is selected to produce the desired current through the erase coil (L_E). The resistor value is calculated:

$$(\text{Total R}) \times (I_E) = V_{OH}(CT_{min}) - V_{OL}(E_{max})$$

For example, with an erase coil resistance of 10 Ω, a desired current of 40 mA, and a supply voltage of 12 volts, R_E is calculated:

$$(R_E + 10) \times (0.04) = 10.5 - 0.6$$
$$R_E = 237.5\ \Omega$$

The power rating of the resistor is:

$$P = (237.5) \times (0.04)^2 = 0.38\ W$$

Thus R_E would be a 240 Ω, ½ watt resistor.

e) Capacitor C_{DG} (Figures 11 and 12) is used only when degauss of the head at the end of writing is desired. This feature is rarely used since the saturation recording pulses produce alternating magnetic polarities, and thus do not generally leave the head magnetized in one polarity. The capacitor value, if needed, can be determined from the graph of Figure 15.

f) The resistors R_D (Figures 11 and 12) are used to dampen any ringing that results from applying the relatively fast risetime write current pulses to the inductive head. Resistor R_P serves as a common pull-up to the head supply voltage. Values chosen for the resistor will depend on the head characteristics, and desired damping.

g) For power-up protection (i.e., to guarantee that no unwanted pulses are written as the power supplies come up), Pin 2 should be held low to disable the head current. Using a capacitor at Pin 2, as described in the data sheet, will provide protection but will also affect the turn-on and turn-off of the head current source relative to $\overline{WG}$ during normal operation. The circuit of Figure 16, however, will hold Pin 2 low during power-up and power-down (when V_{CC} is less than +4.0 V), but will not affect normal operation.

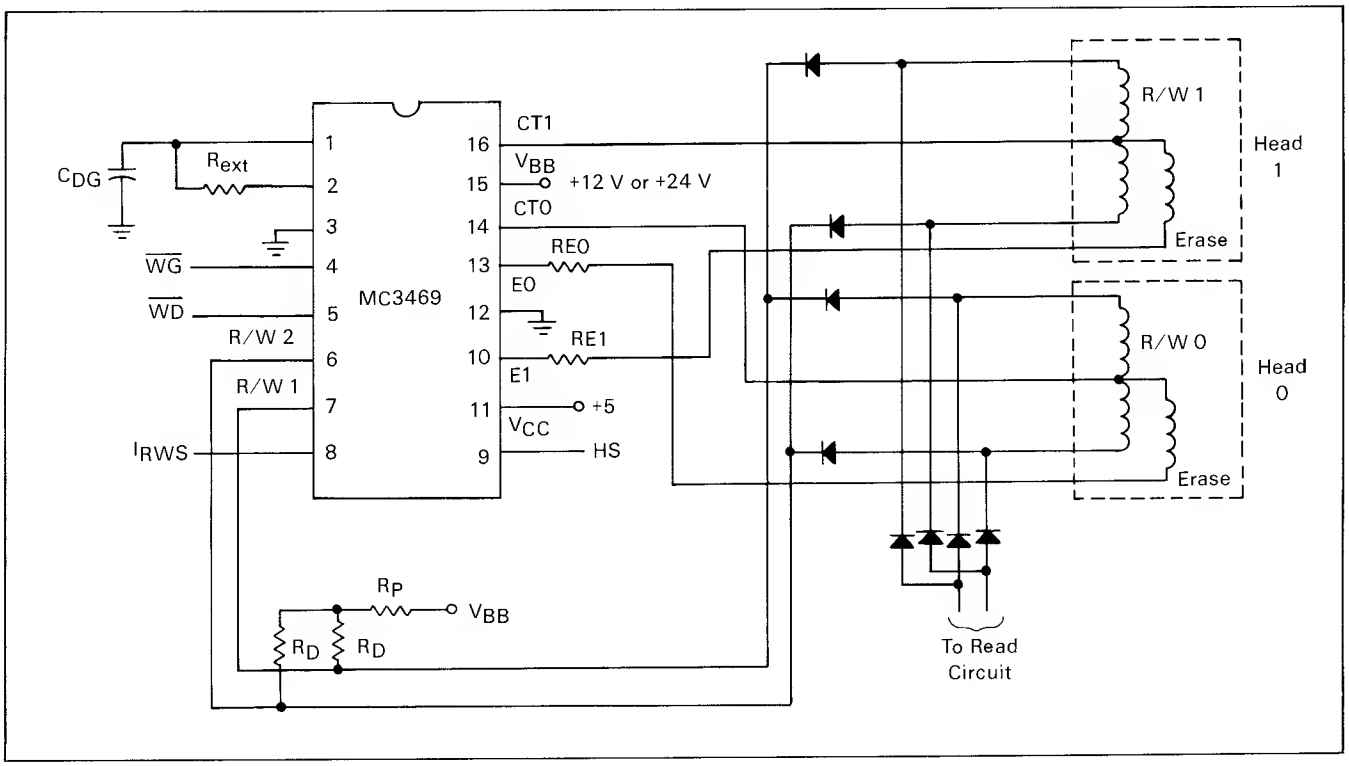


FIGURE 11 — Typical Application of MC3469

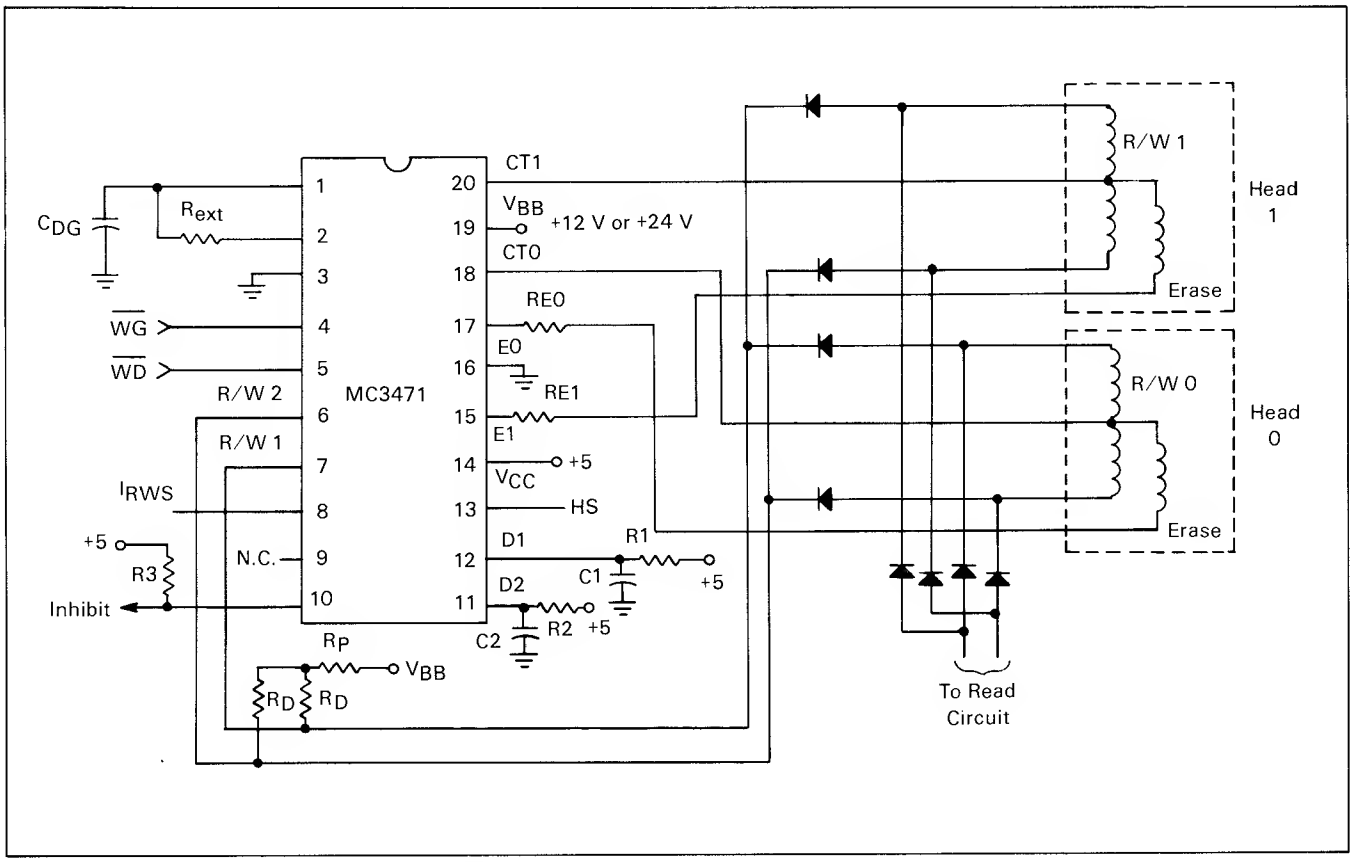


FIGURE 12 — Typical Application of MC3471

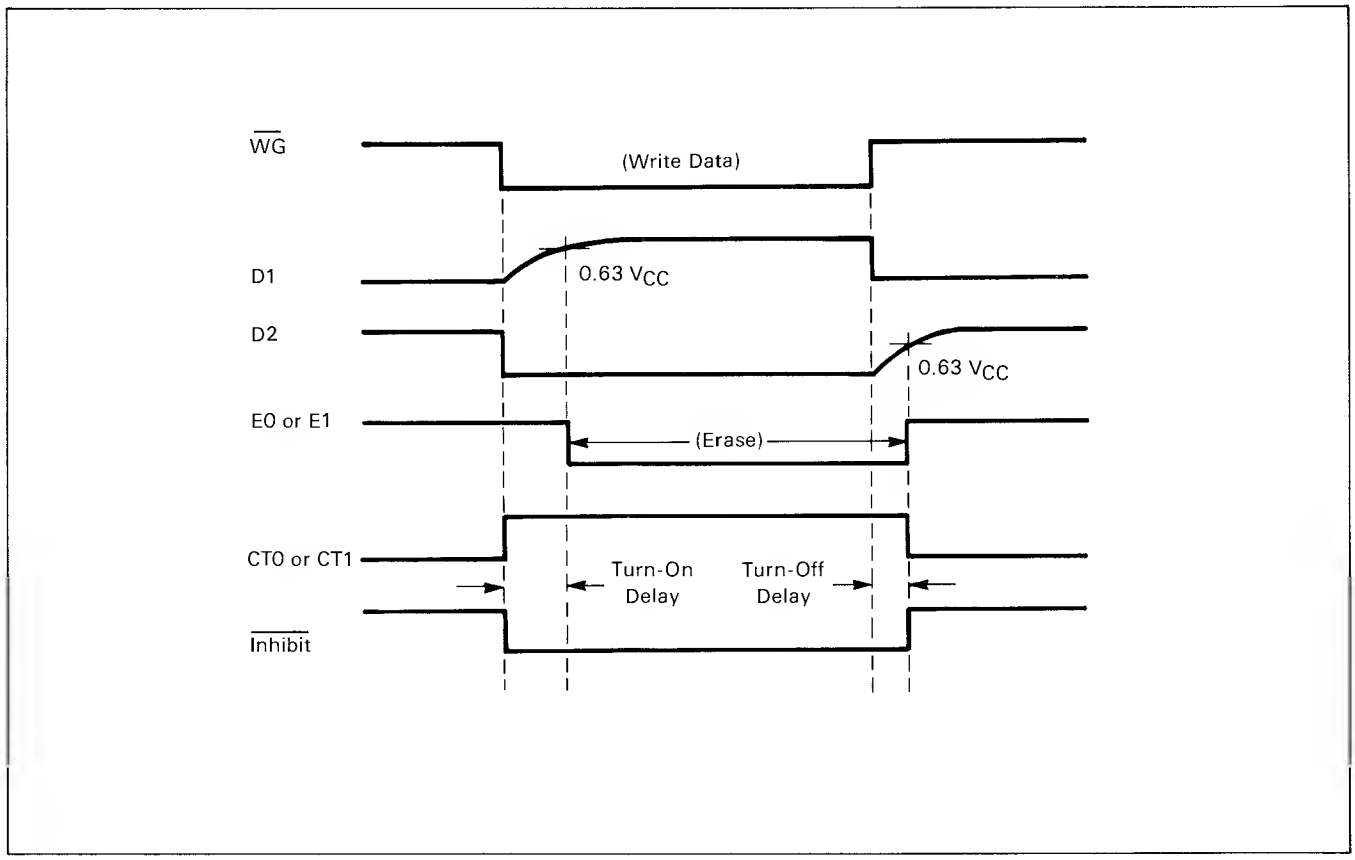


FIGURE 13 — RC Control of Erase Delays (MC3471)

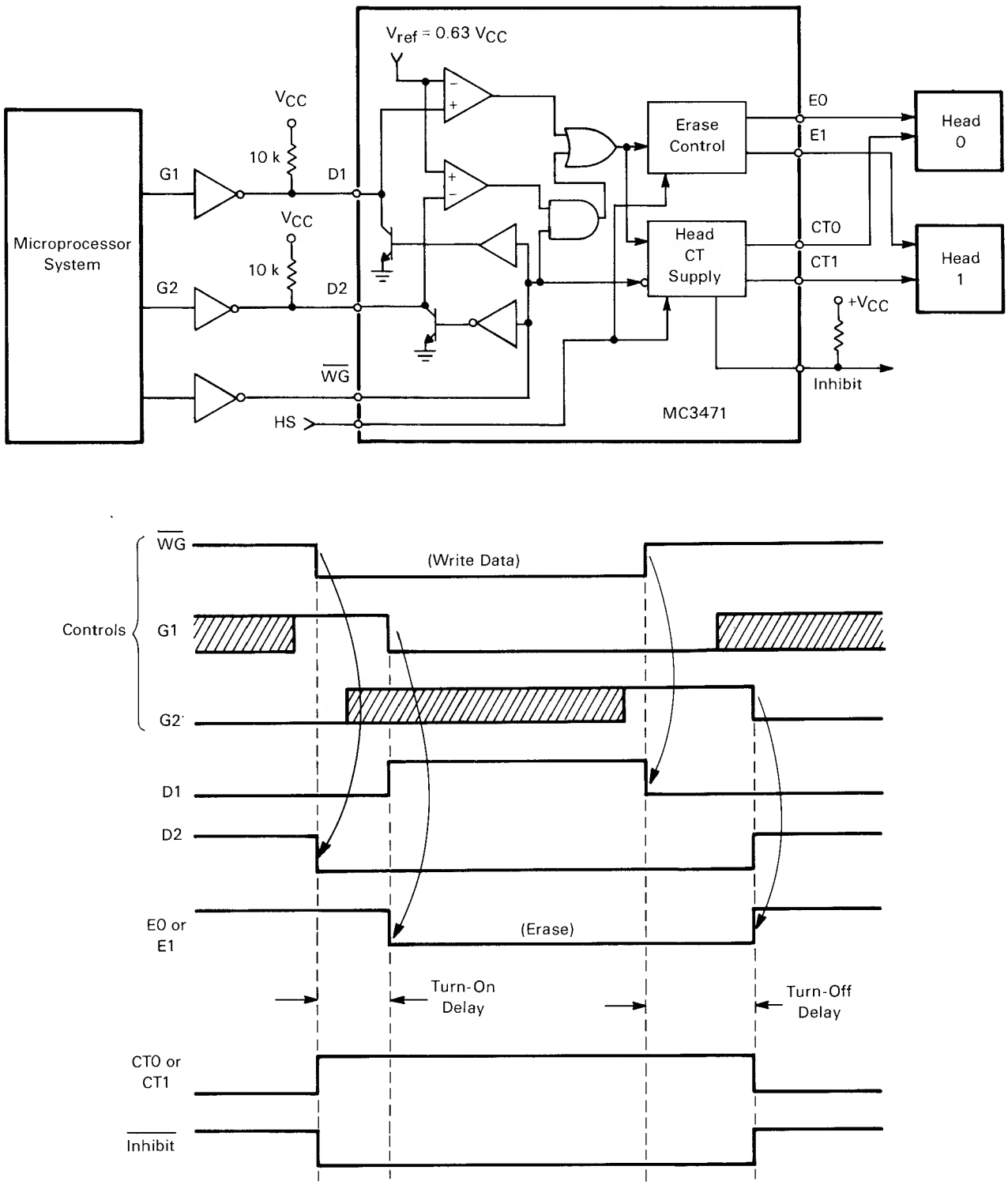


FIGURE 14 — External Gate Control of Erase Delays (MC3471)

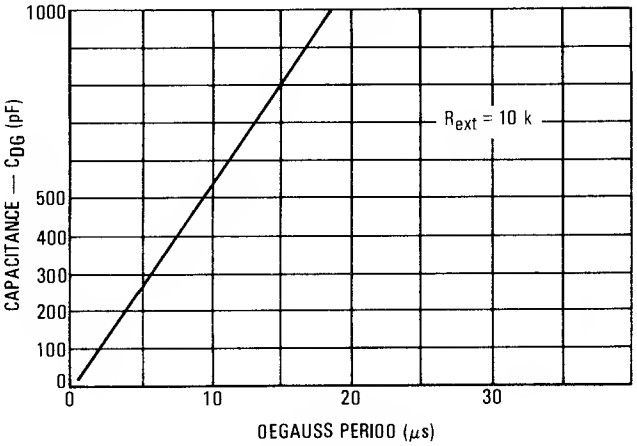


FIGURE 15 — Degauss Period versus C_{DG}

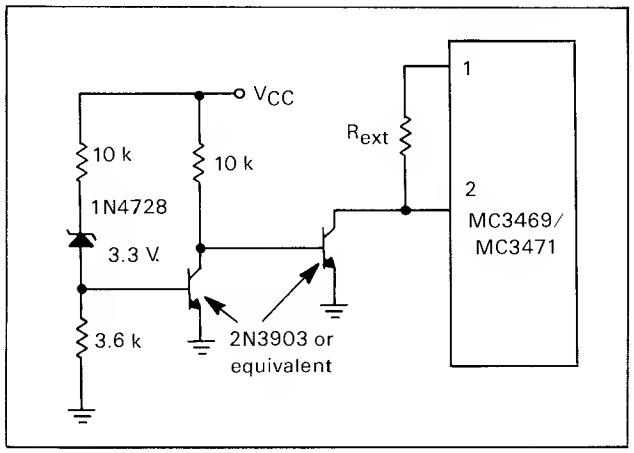


FIGURE 16 — Power-On Protection

READ AMPLIFIER CIRCUIT — MC3470/MC3470A

The MC3470 is designed to accept the differential ac signal from the magnetic head of a floppy disk drive, and provide at the output (Pin 10) pulses which correspond to the peaks (+ and –) of that ac signal. Referring to Figure 17, the preamplifier boosts the signal by a factor of approximately 100, and applies it to the external filter network. The filtered waveform is then used by the active differentiator, comparator, and time domain filter to produce a digital output. A description of the various sections follows.

HEAD CONNECTIONS

Three methods of connecting the MC3470 to the Read/Write head are shown in Figure 18. The circuit in Figure 18(a) is the simplest and least expensive, but leaves the read circuit subject to a switching transient when the system is switched from a write operation to a read operation. As the head center tap (CT) is switched from V_{BB} (+12 V or +24 V) to ground, the diodes are switched from a reverse bias condition to a forward bias condition, and any difference in the diodes' capacitance will cause a non-symmetrical common-mode transient to appear at the inputs, and outputs, of the MC3470 amplifier. The differential output waveform of the amplifier is shown in Figure 19(a) (the output, during "read", is a 250 kHz signal supplied from the R/W head). The switching response is also affected by any mismatch in the two halves of the R/W head, head wiring, and any temperature difference in the diodes (they should be adjacent to each other).

If the system cannot wait for the transient to settle out, the circuit of Figure 18(b) can be used. The adjustment will compensate for all mismatches, and transients will not appear during the switching [see Figure 19(b)]. The circuit of Figure 18(c) eliminates the need for the adjustment since the FETs (Q1 and Q2) isolate the read circuit from the R/W head during writing. When switching to a read operation, the head center tap is first switched to ground, then the FETs are turned on.

System timing, and cost objectives will determine which circuit is most appropriate.

PREAMP CHARACTERISTICS

The MC3470 preamplifier is a differential-input, differential-output amplifier, with a typical gain of 100 V/V (110 V/V for the MC3470A). The input common-mode range is -0.1 V to +1.5 V, a range which generally does not present a problem when the input and head are wired as shown in Figure 18. Note that the read head circuitry must be capable of sinking the input bias current (10–25 μA).

The output (Pins 16 and 17) has a common mode level of $\simeq$ 3.0 V, which is essentially independent of the input common mode voltage, and of V_{CC2} (+12 V) variations. V_{CC1} (+5.0 V) variations, however, will cause the output common mode level to shift by ap-

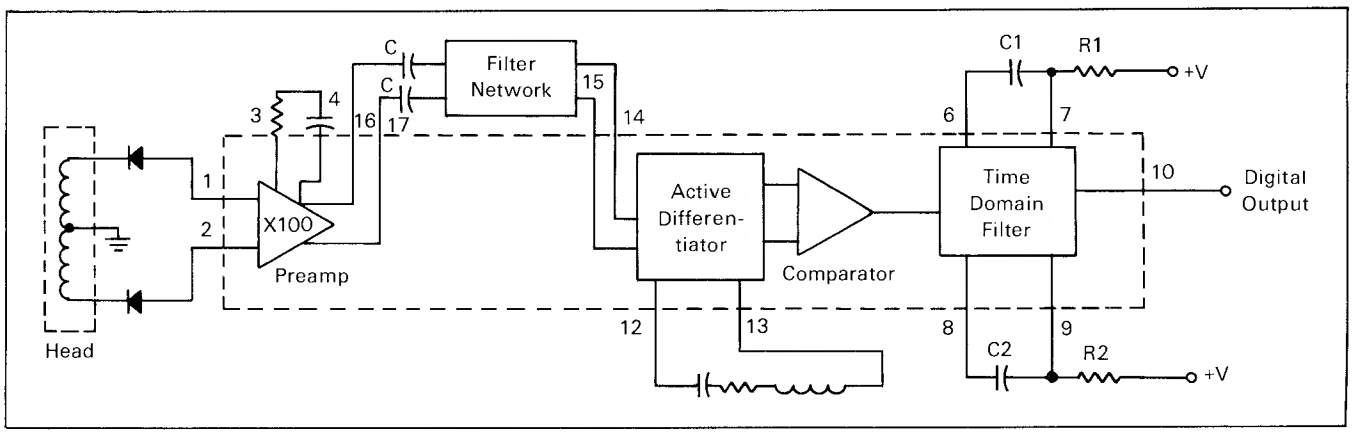


FIGURE 17 — MC3470 Read Amplifier

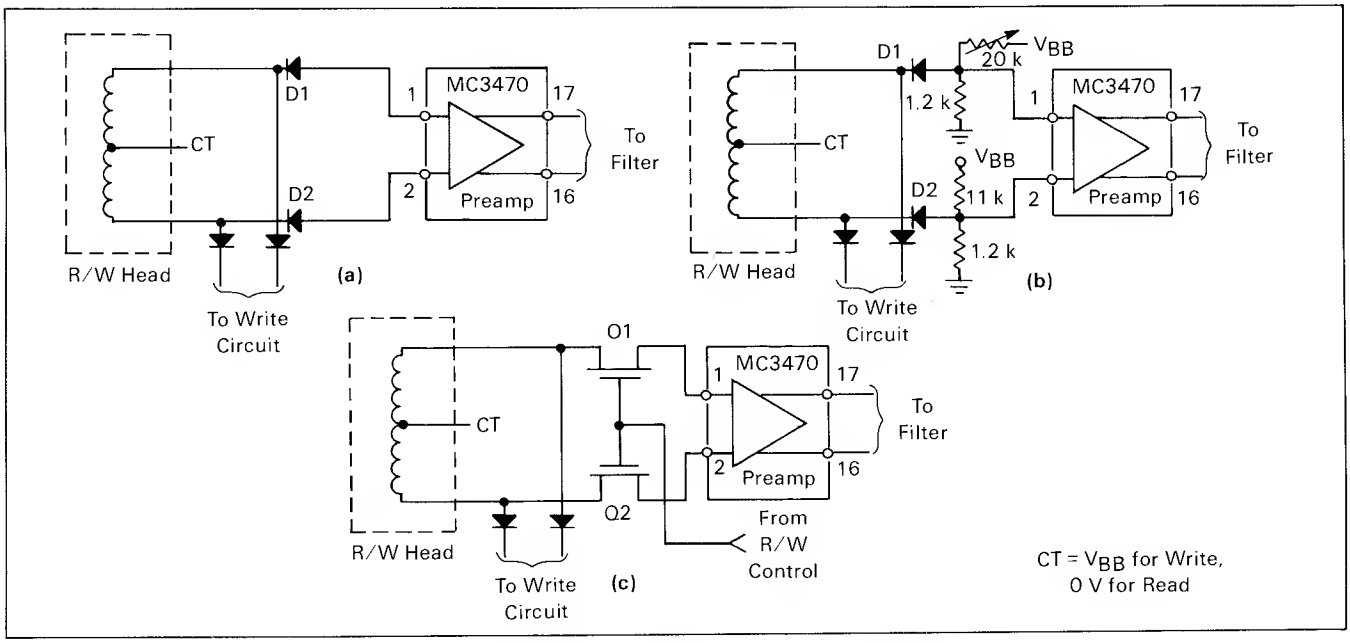


FIGURE 18 — Coupling R/W Head to the MC3470

proximately 90% of the V_{CC1} change. Since the output signal is typically ac coupled to the next circuit, any common-mode shift generally does not present a problem. The output **differential** is the signal of interest, and does not vary by more than 0.3% (-50 dB) with respect to either power supply voltage.

Distortion in the output signal increases if the output swing exceeds 3.0 Vp-p (the output clips at 4.0 Vp-p). If the input signal is expected to exceed 25 mVp-p, the gain should be reduced appropriately. Pins 3 and 4 provide access to an intermediate stage of the preamp where the gain, as well as the low frequency roll-off, may be controlled. See Figure 20 for typical frequency response curves. The gain (in the flat portion of each curve) is controlled by the resistor according to:

$$A_{VR} = A_{VO}\left(\frac{500}{R + 500}\right)$$

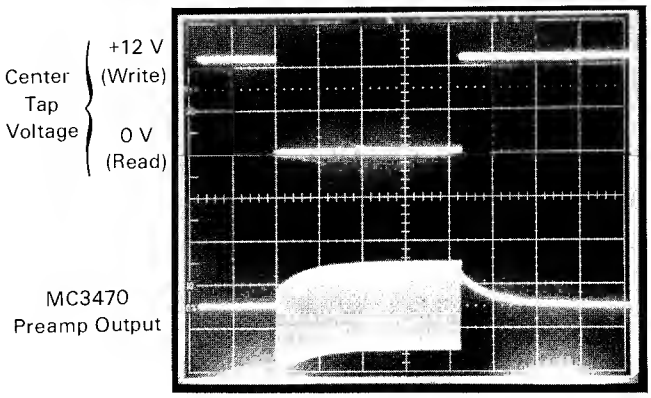
where A_{VR} = the reduced gain;
A_{VO} = the gain with R=0 (typically 100 V/V);
R = the external resistor (in ohms).

The capacitance C, in conjunction with the above calculated resistor, will determine the low frequency roll-off. The -3.0 dB point will be at approximately:

$$f = \frac{1}{2\pi C(R+500)}$$

If Pins 3 and 4 are connected together (no R,C), the gain will be flat down to dc. The drawback in doing this lies in that an offset voltage may appear at the input, either from the signal source or from internal drift, which will show up at the output (amplified, of course). The capacitor blocks the input offset, and passes only the ac portion of the signal.

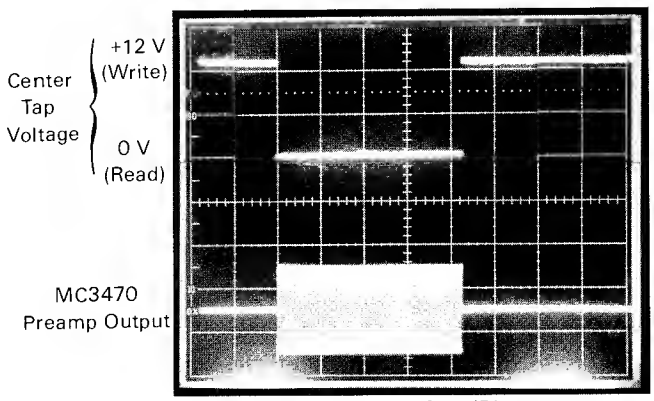
An inductor could be added, in series with an appropriately chosen resistor and capacitor, to reduce high frequency gain, thus producing a band-pass filter. Since Pins 3 and 4 are at an intermediate stage of the preamp, however, noise coupled into the output from the MC3470's digital section (Pins 6 through 10) would not be attenuated by these components. For this reason, high frequency roll-off is best left to a low-pass filter at the preamp output (see next section).



Horizontal = 100 μs/Div

Switching Transient Due to Diode Mismatch

(a)



Horizontal = 100 μs/Div

Diode Mismatch Adjusted Out

(b)

FIGURE 19

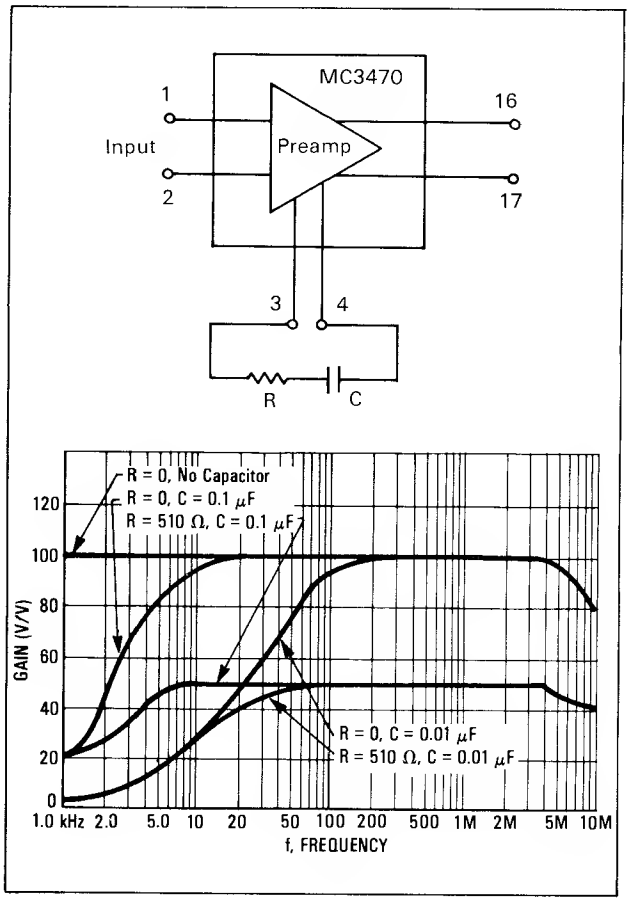


FIGURE 20 — Preamp Gain Characteristics

FILTER CONSIDERATIONS

The filter network's purpose is to remove high frequency noise present on the amplified signal so as to present a clean signal to the differentiator. The noise sources are varied, and include media/head characteristics, noise pick-up on the head wiring, and effects of digital circuitry on the sensitive preamp stage. Design of the filter requires consideration of many factors, some of which are:

- Preamp output stage characteristics;
- Differentiator input stage characteristics;
- Data transfer rate;
- Read head characteristics;
- System transient response;
- Noise characteristics;
- Desired frequency characteristics;
- Insertion loss.

Filter criteria varies among disk system manufacturers, consequently filter designs vary. Since the filter has a differential input and output, most designs consist of a balanced configuration.

The filter design must consider the current-sinking capability of the amplifier output. A current source in the output structure is guaranteed to sink a minimum current of 2.8 mA. If the input current requirements of the filter exceed 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator/comparator. Therefore, the total impedance looking into the filter must be greater than Z_{min} as calculated by:

$$Z_{min} = \frac{(E_p) \times (A_{vd})}{2.8\ mA}$$

where E_p is the peak differential voltage from the head, and A_{vd} is the gain of the preamp.

The differentiator inputs have an internal biasing network (2.5–3.0 V). Any dc voltage applied to these inputs will perturb the bias level which in turn will cause an incorrect digital output. Since the output of the preamp also has an associated dc voltage level (≈3.0 V), it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. Optimum transient response results if the requirement for blocking capacitors is limited to the input of the filter (as shown in Figure 17). The charging and discharging of C and C′ are then controlled by the filter's input impedance rather than the high input impedance of the differentiator.

FILTER EXAMPLE

Figure 21 depicts a typical filter that can be used in an 8 inch floppy disk drive. It is a balanced low-pass PI filter, with an insertion loss of about 6.5 dB. The -3.0 dB point is at 850 kHz, so that the 500 kHz required for MFM reading is easily passed. This same filter could be used for a 250 kHz transfer rate. However, improved performance will result with a filter designed to produce a -3.0 dB point at 375 kHz.

TIME DOMAIN FILTER

Purpose

The timing diagram of Figure 22 depicts some of the waveforms encountered in the circuit of Figure 17. After the input signal is amplified, and filtered, it is then differentiated (to change the peaks to zero-crossings) and applied to the comparator. The comparator output toggles each time its inputs sense a zero crossing. The comparator output is then applied to the time-domain filter, which has a dual purpose. The primary purpose is to generate an output pulse (at Pin 10) for each transition of the comparator output. These pulses correspond to valid data read off the disk. The second purpose is to filter out false zero crossings which can be caused by noise during the "shouldering" period as shown in the second trace of Figure 22. Shouldering is a result of media characteristics and recording format, and can be aggravated by media defect and contamination. For example, formats which permit excessive distances between bits can generate shouldering situations, by allowing the read signal to droop and possibly create a false zero crossing. Filtering out false information involves the use of an "ignore window", during which time any zero crossings are ignored. A description of how this is accomplished follows.

Description

The MC3470 time-domain filter consists of a pulse generator, two one-shots, and a D-type flip-flop (depicted in Figures 23 and 24). Each transition of the comparator output causes the pulse generator to provide a trigger pulse to the first one-shot, T1, which provides the ignore window (time t1 in Figure 24). When

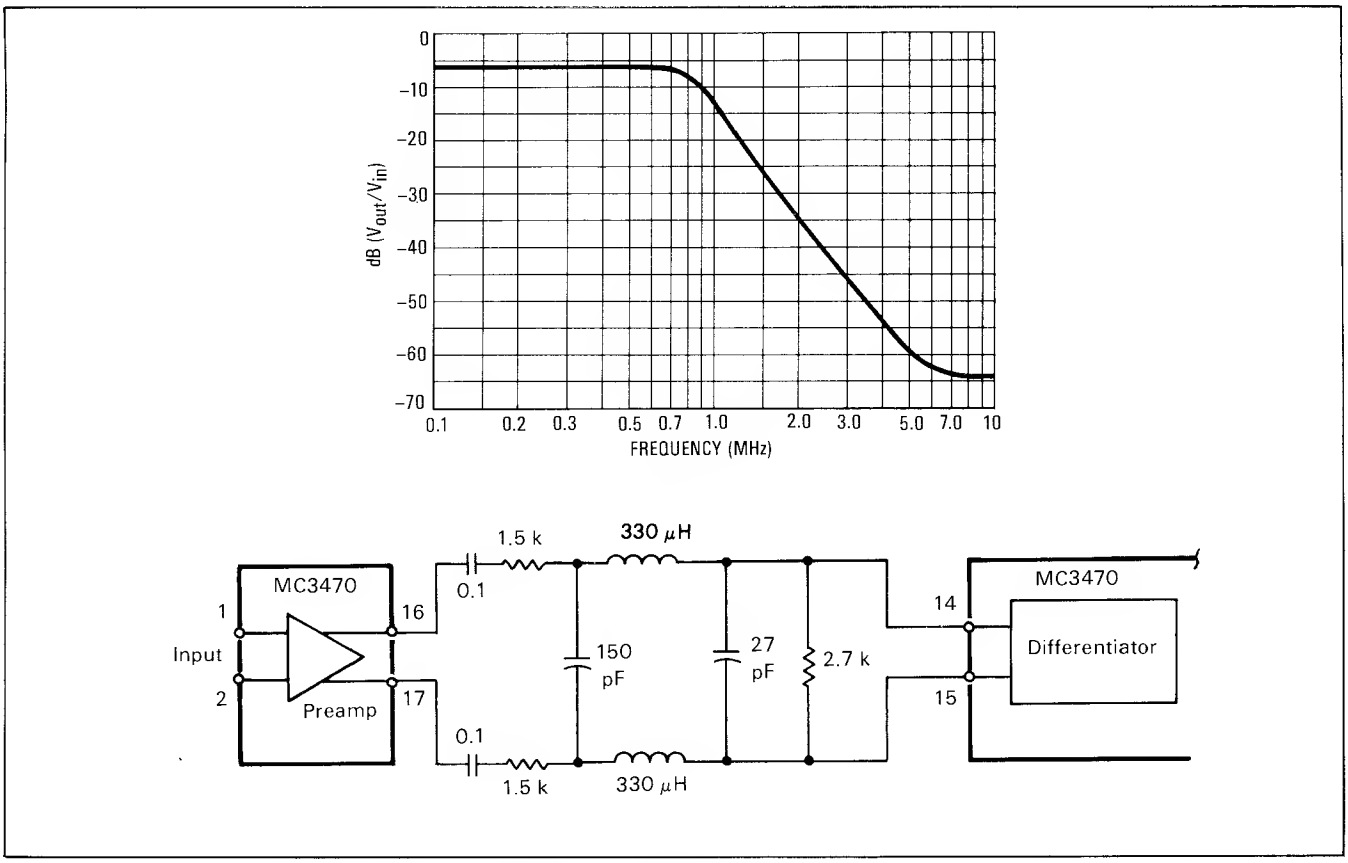


FIGURE 21 — Filter Example (8 in. Drive)

the T1 output returns to the normal level (low-to-high transition), the D-type flip-flop clocks through the new data (from the comparator), causing the Q and $\overline{Q}$ outputs to switch. This in turn triggers the second one-shot, T2, to produce an output pulse. Note, however, that T2 will be triggered only if the comparator output has changed, and remained at the new level, from the last clocking of the D-type flip-flop. If, however, the comparator changed level due to shouldering (or noise) and returns to its original level within the t1 period, the D-type flip-flop outputs will not change, and T2 will not generate a new output pulse.

As a result of the above described sequence, the T2 output pulses will be delayed from the peaks of the input signal by an amount equal to t1 (see Figures 22 and 24).

The expected distortion time (ΔT) must be determined by the disk drive designer, as this will depend on the data transfer rate, head characteristics, and media characteristics. Additionally, the time T_A in Figure 24 (the time from a peak to the beginning of the distortion time) should be determined so as to be able to set t1 to **not** time out during ΔT. If this were allowed to happen, the circuit will fail to produce the valid output pulses immediately before and after ΔT. The time period t1 should be chosen according to the following guidelines:

- $t1 > \Delta T$
- $t1 < T_A$ **or** $t1 > T_A + \Delta T$
- $t1 < 0.7T_B$
- $0.5\ \mu s < t1 < 4.0\ \mu s$

The time period t1 is determined by R1 and C1 according to the equation: $t1 = [(0.625)(R1)(C1) + 200\ ns]$ ($1.5\ k\Omega \leqslant R1 \leqslant 10\ k\Omega$, $150\ pF \leqslant C1 \leqslant 680\ pF$). C1 should be chosen to be as small as practical to minimize internal current transients.

The output pulse width (t2) depends on the requirements of the host controller, and is determined by R2 and C2 according to the equation: $t2 = [(0.625)(R2)(C2)]$ ($1.5\ k\Omega \leqslant R2 \leqslant 10\ k\Omega$, $100\ pF \leqslant C2 \leqslant 800\ pF$). C2 should be as small as practical to minimize internal current transients.

Both of the above time periods (t1 and t2) are guaranteed accurate to ±15%.

NOTE: In the absence of a signal from the head to the read channel, such as during a write operation, noise may enter the MC3470 through the differentiator pins, causing one-shot T1 to trigger in a random manner. One-shot T2 will also trigger, with additional randomness, causing spurious output pulses. The pulses should be gated out by the disk drive, or ignored by the controller, since they are obviously meaningless.

The above described condition is more noticeable if the circuit design involves the use of a potentiometer (see Figure 26) to correct for peak-shift (which is discussed in the next section). With the potentiometer in place and adjusted, offset at the comparator inputs is essentially nulled decreasing the noise amplitude required to switch the comparator. Removing the potentiometer results in a higher noise level required to switch the comparator due to the comparator's offset. However, since the above situation exists only during non-read operations, it should not present a problem in most applications.

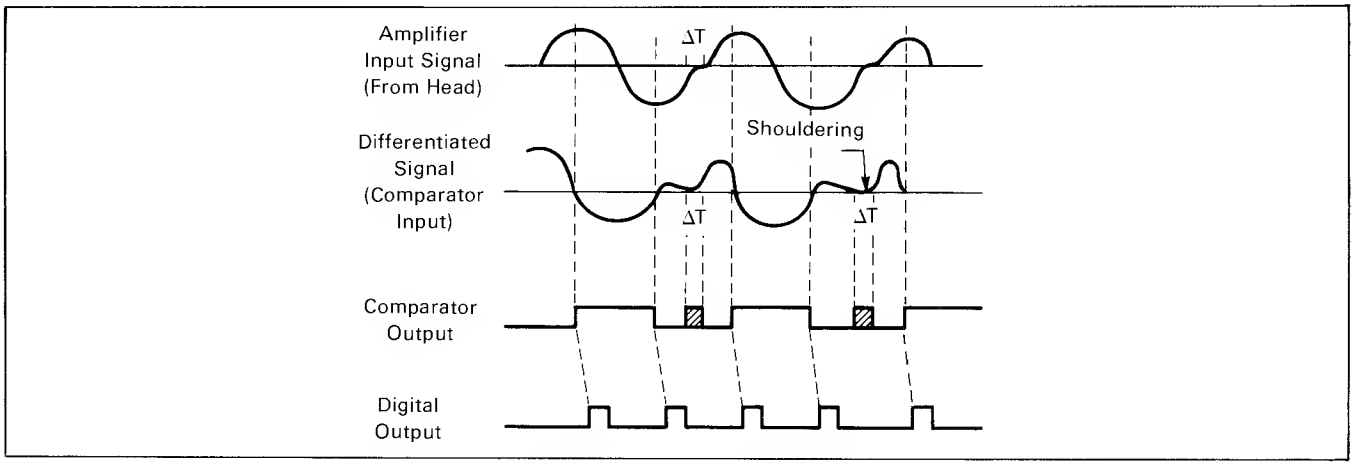


FIGURE 22 — Read Signal Waveforms

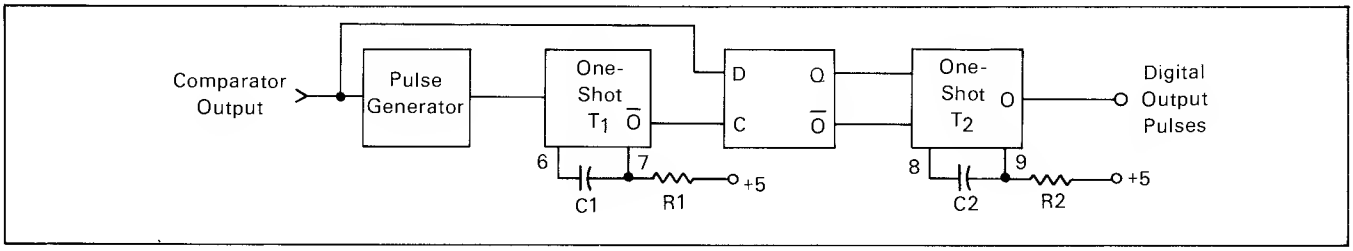


FIGURE 23 — Time Domain Filter Components

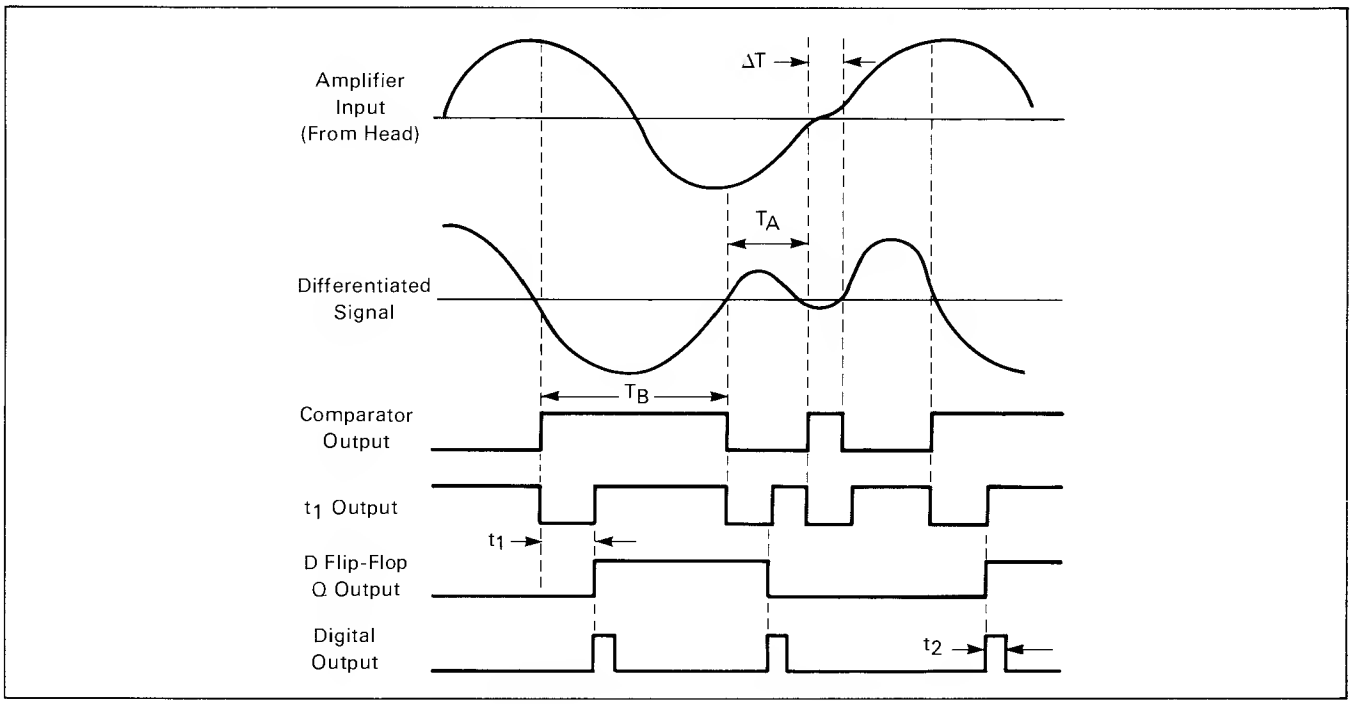


FIGURE 24 — Time Domain Filter Timing

PEAK SHIFT CONSIDERATIONS

Among the many considerations involved in reading data from a disk is the requirement that the timing of the output pulses be consistent. The timing accuracy is not only a means of verifying the validity of the data and of the disk system operation in general, but is also necessary for proper operation of the host controller. In order for the host controller to synchronize itself with the data stream coming from the disk at the beginning of each read operation, a phase-locked loop circuit is generally used. If the data bits (out of the MC3470) are not supplied at a consistent rate, the host will either reject some data pulses as non-valid, or will lose synchronization and all data thereafter.

In an ideal system, data bits are written onto the disk with no timing errors, and then the bits are read, amplified, differentiated, and converted to pulses at a perfectly consistent rate. Since ideality is generally lacking in most systems, data pulses are supplied from

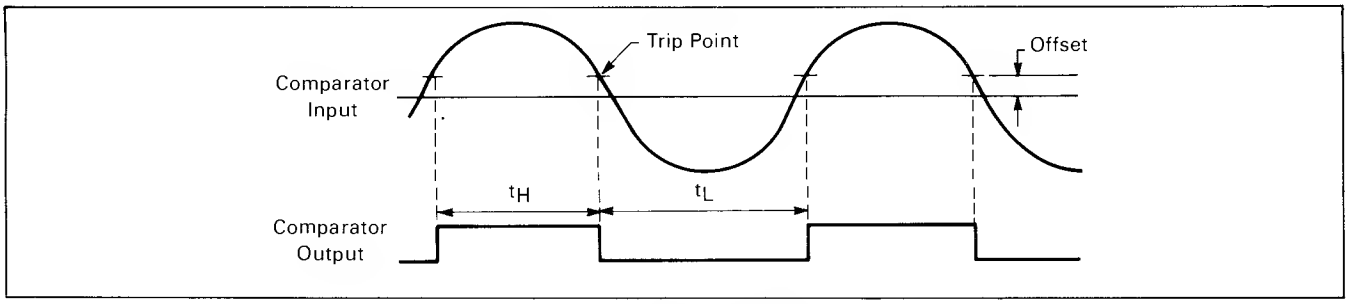


FIGURE 25 — Comparator Offset

the read channel at slightly varying intervals, a problem referred to as peak-shift. The problem has several causes, including incorrect timing during writing, non-symmetrical characteristics of the read head, preamplifier, filter and differentiator, offset and speed response of the zero-crossing detector (comparator), and noise. Relative to the MC3470, the two main causes of peak-shift are noise, and comparator offset.

Noise can enter the IC through several of its pins, and so care is required in the PC board layout. A ground plane directly underneath the IC, and for some distance around it (to whatever extent possible) is always necessary. The ground plane should not be routed through a maze of digital circuitry, but should be connected to the power supply ground by the shortest and most direct means possible. The input signal, having only a few millivolts of amplitude, should have a short and direct path from the head, and should not pass near any digital circuitry or motor wiring. All components (such as the low-pass filter, and the RC networks) should be located physically adjacent to the IC.

In addition to the above commonly employed PC board techniques to reduce noise effects (particularly with low output heads), some precautions specific to the MC3470 are worth noting:

a) Noise (sufficient to cause errors) will appear at the output of the preamp at each transition of the internal one-shots, due to inherent coupling within the IC. A well designed low-pass filter (Pins 14 through 17), will block the spikes and present a clean signal to the differentiator.

b) If the RC networks (Pins 6 through 9) are located more than 2″ from the IC, the one-shots may oscillate during their respective time-out. As mentioned above, these components should be physically adjacent to the IC.

The zero-crossing detector must provide an output transition when the inputs cross the zero-point (exactly) — switching at any other point (offset) results in incorrect output timing, as shown in Figure 25. In this figure, t_H is obviously not equal to t_L, and the output pulses (Pin 10) will have the same non-symmetrical timing. Comparator offset is easily nulled by connecting a potentiometer to Pins 12 and 13, as shown in Figure 26.

The pot is then adjusted for minimum peak shift at Pin 10. This configuration allows for adjustment of peak shift contributed by both internal and external sources. Neglecting external sources, unadjusted peak shift (without the potentiometer) is guaranteed to be $<\pm 2\%$ for the MC3470A.

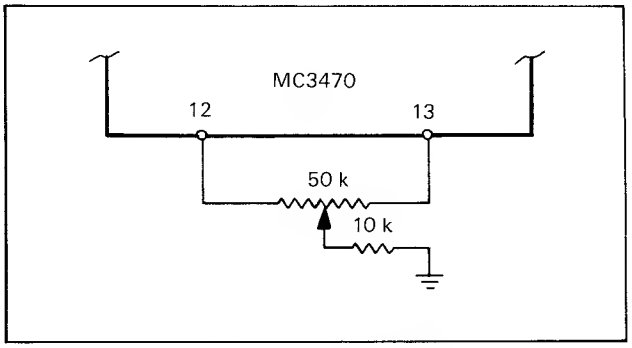


FIGURE 26 — Offset Adjustment

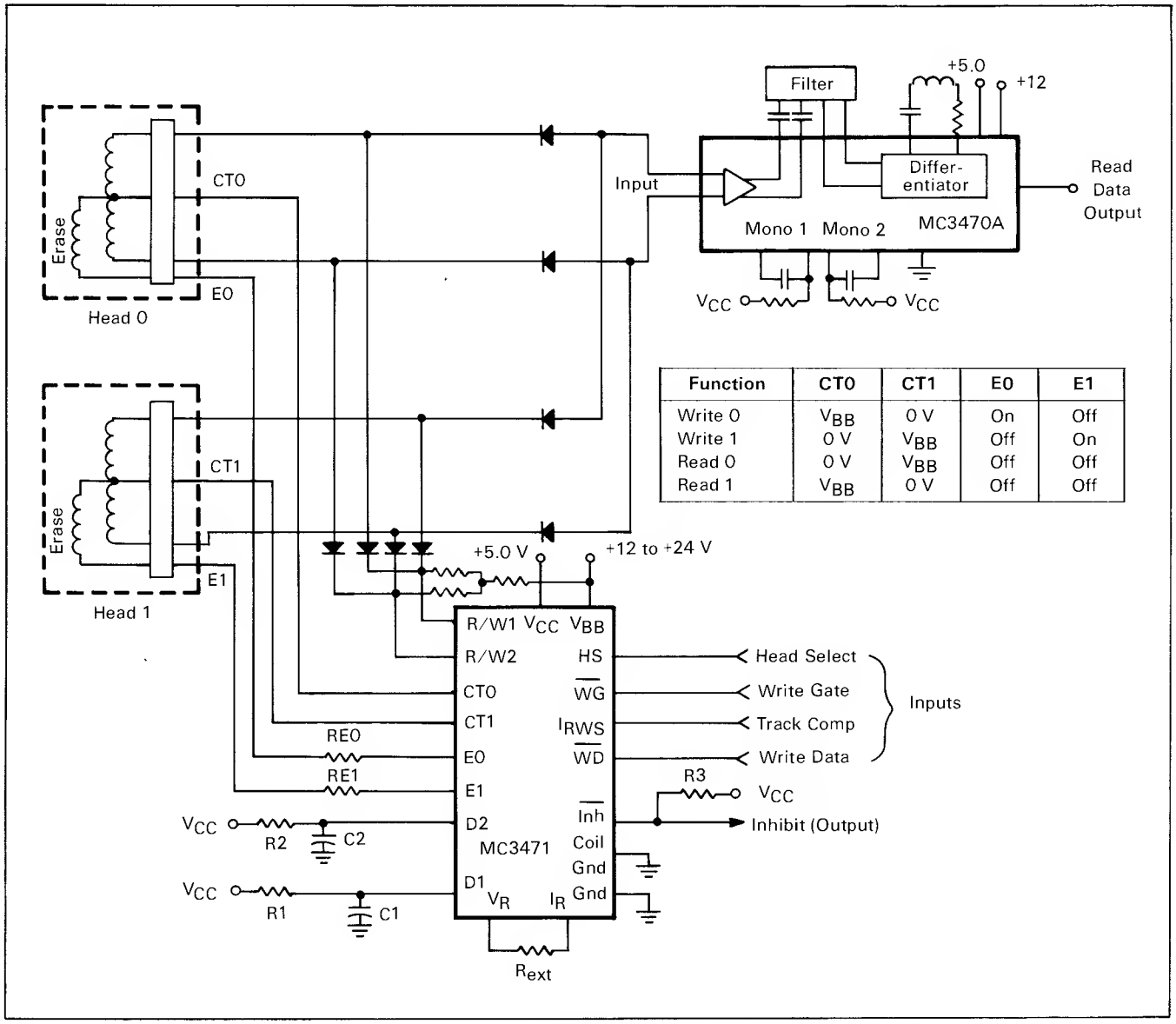
Speed response of the comparator is primarily dependent on the slew rate of the signal at its inputs. Since the gain of the comparator is finite, rather than ideal, the comparator has a linear operating region of about 150 μV (at the inputs). The quicker the input signal passes through this region, the less uncertainty at the output, and a sharper transition results. More importantly, a high slew rate provides, in a shorter time, the overdrive necessary to ensure the fastest and most consistent propagation delay. While propagation delay itself does not add to peak shift, it is easy to see that if the delay encountered when switching high-to-low is different than for switching low-to-high, peak shift will be affected. The designer of the floppy disk system should therefore strive for the highest possible amplitude (within the device limits) at the input of the differentiator (Pins 14 and 15), in order to provide the highest slew rate at the comparator inputs.

COMPLETE READ/WRITE CIRCUIT

A complete read/write circuit for a two-head system is shown in Figure 27, employing the MC3470 and MC3471. The table indicates the various output levels, in response to the desired function, which is determined by $\overline{WG}$ and HS. Some variations of this circuit include:

- The MC3469 could be used, in place of the MC3471, for straddle erase heads, thus eliminating R1, R2, R3, C1, and C2.
- FET switches (discussed previously) could be used in place of the diodes, as shown in Figure 28. Control of the FET gates would be accomplished by appropriately gating the Head Select and $\overline{\text{Write Gate}}$ signals to provide the R/W control.

Other variations of the circuit shown are possible. Each designer must determine individual circuit requirements based on specific head characteristics, data transfer rates, disk bit densities, and other factors.



Function	CT0	CT1	E0	E1
Write 0	V_{BB}	0 V	On	Off
Write 1	0 V	V_{BB}	Off	On
Read 0	0 V	V_{BB}	Off	Off
Read 1	V_{BB}	0 V	Off	Off

FIGURE 27

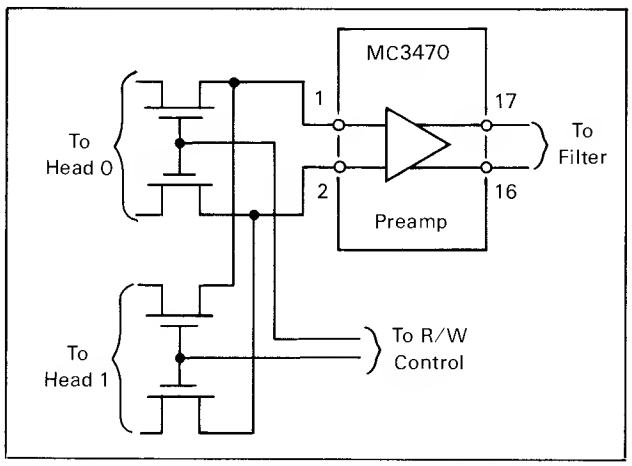


FIGURE 28 — Using FETs To Isolate the Read Channel

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